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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/912,768	07/24/2001	James Shutt	CYPR-CD00200	5143

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EXAMINER	
SURYAWANSHI, SURESH	

ART UNIT	PAPER NUMBER
2115	

DATE MAILED: 04/11/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/912,768	SHUTT, JAMES	
	Examiner	Art Unit	
	Suresh K Suryawanshi	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/2/05 amenedments*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9 and 11-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9 and 11-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 July 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-9 and 11-27 are presented for examination.

Drawings

2. This application, filed under former 37 CFR 1.60, lacks formal drawings (Fig. 3 and 4). The informal drawings filed in this application are acceptable for examination purposes. When the application is allowed, applicant will be required to submit new formal drawings. In unusual circumstances, the formal drawings from the abandoned parent application may be transferred by the grant of a petition under 37 CFR 1.182.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5 and 19-22 are rejected under 35 U.S.C. 102(b) as being anticipated by Schade, Jr. (US Patent No 4,250,464; hereinafter referred to as Schade).

5. As per claim 1, Schade teaches an oscillator circuit comprising:

a relaxation oscillator circuit [Fig. 1; col. 1, lines 22-29; the oscillator 14];

a first current oscillator for establishing a first reference voltage for use in causing said relaxation oscillator circuit to operate in a first power mode to generate a clock of a first accuracy [Fig. 1; col. 2, lines 28-47; current source 24 that provides a larger current];

a second current source for establishing a second reference voltage for use in causing said relaxation oscillator circuit to operate in a second power mode to generate a clock of a second accuracy, wherein said first current source is not operable to establish said second reference voltage [Fig. 1; col. 1, lines 49-64; current source 18 that provides a low magnitude current; during normal mode operation, the current source 24 is kept off through switching means 26]; and

a control coupled to said first current source and said second current source for switching between said first power mode and said second power mode [Fig. 1; col. 2, lines 28-47; switch means 26 for controlling current flow from the current source 24 to the capacitor 16].

6. As per claim 19, Schade teaches that in a relaxation oscillator circuit having a first current source for a first power mode and a second current source for a second power mode [Fig. 1; col. 2, lines 28-47; current source 24 that provides a larger current; col. 1, lines 49-64; current source 18 that provides a low magnitude current], a method for generating clock signals comprising the steps of:

selecting a switch current source [Fig. 1; col. 2, lines 28-47; switch means 26 for controlling current flow from the current source 24 to the capacitor 16];

generating a reference voltage based on said switched current source [Fig. 1; col. 2, lines 28-47; switch means 26 for controlling current flow from the current source 24 to the capacitor 16]; and

in response to said reference voltage, using said relaxation oscillator circuit to generate a clock signal having an accuracy that depends on said present power mode [Fig. 1; col. 1, lines 13-17, 22-29, 49-64; col. 2, lines 28-47; two modes of operations - standby and alarm and alternatively low power mode and high power mode].

7. As per claims 2 and 20, Schade teaches that first current source supplies a larger current than said second current source [Fig. 1; col. 1, lines 59-64; col. 2, lines 28-47].

8. As per claim 3, Schade teaches that first reference voltage is established across a resister [Fig. 1, 2; switch means].

9. As per claim 4, Schade teaches that second reference voltage is established across a diode-connected field effect transistor [Fig. 1; discharge means 20].

10. As per claim 5, Schade teaches that the oscillator circuit further comprising trimmable current sources [col. 3, lines 38-49].

11. As per claims 21 and 22, Schade discloses that first power mode is a low power mode and second power mode is a very low power mode [col. 1, lines 59-64; col. 2, lines 28-47].

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

13. Claims 6 and 23-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schade, Jr. (US Patent No 4,250,464; hereinafter referred to as Schade) in view of May (US Patent No 5,426,384).

14. As per claims 6 and 23, Schade discloses the invention substantially. Schade does not disclose about trimmable current sources are being digitally controlled. However, May clearly discloses the knowledge of a voltage-controlled oscillator (VCO) having a voltage controlled current source that is digitally controlled. May also discloses that the VCO could be replaced by a relaxation oscillator [col. 5, liens 56-59; col. 9, lines 5-7]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed to voltage controlled oscillator. Moreover, a digitally controlled current source can be controlled by a microcontroller or microprocessor. A digitally controlled current source is less susceptible to changes caused by environmental conditions.

15. As per claim 24, Schade discloses that relaxation oscillator circuit comprises four trimmable current sources [col. 3, lines 38-49].

16. Claims 7-8 and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schade, Jr. (US Patent No 4,250,464; hereinafter referred to as Schade).

17. As per claims 7-8 and 25-27, Schade discloses the invention substantially. Schade does not expressly disclose that first current generates a current of 2 micro amps and second current source generates a current of 100 nano amps. However, Schade clearly discloses that the clock frequency of the first operating mode being lower than the clock frequency of the second operating mode [col. 1, lines 22-29, 49-64; col. 2, lines 28-47]. Therefore, it would have been obvious to one of ordinary skill in the art at time the invention was made to have the first current source generating a current of 100 nano amps and second current source generating a current of 2 micro amps.

18. Claims 9, 11-13, 16-18, are rejected under 35 U.S.C. 103(a) as being unpatentable over Nolan et al (US Patent no 6,052,035[1]) in view of Schade, Jr. (US Patent No 4,250,464; hereinafter referred to as Schade)

19. As per claim 9, Nolan et al teach

a bus [use of a bus in a computer system is inherent and clearly the circuit of relaxation oscillator in Fig. 3 is used in a computer system];

a processor coupled to said bus [a processor coupled to a bus is inherent in a computer system and clearly the circuit of relaxation oscillator in Fig. 3 is used in a computer system];

a memory unit coupled to said bus [a memory unit coupled to a bus is inherent to a compute system and clearly the circuit of relaxation oscillator in Fig. 3 is used in a computer system];

a plurality of input/output pins [a processor or a memory unit in a computer system having input/output pins is inherent and clearly the circuit of relaxation oscillator in Fig. 3 is used in a computer system]; and

[1] Prior art cited by examiner in the prior office action (dated 6/15/04).

a time circuit coupled to said bus for performing a timing function, said timer circuit comprising a relaxation oscillator circuit having a first power mode and a second power mode, said first power mode and said second power mode being switchable under a control [col. 8, lines 48-63; a timing capacitor performing a timing function; first operating mode and second operating mode of the relaxation oscillator; operating mode is switchable under selection of a resistor],

wherein said relaxation oscillator circuit comprises:

a first current source [Fig. 3; col. 3, line 14; a first current generator 200];

a second current source [Fig. 3; col. 3, line 16; a second current generator 300].

Nolan et al do not disclose that the first current source and the second current source supply the current independent of each other as Nolan et al teach that the two current generators work in combination to generate a summed current. However, Schade expressly discloses about a relaxation oscillator circuit having a first current source and a second current source independent of each other and having a switch means to control the switching between them [Fig. 1; col. 1, lines 22-29, 49-64; col. 2, lines 28-47; col. 3, lines 38-49]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as both are directed towards a dual mode relaxation oscillator. Moreover, a routineer would utilize the disclosed relaxation oscillator circuit by Schade for it's simple design and less cost effectiveness.

20. As per claim 11, Nolan et al teach that wherein said first current source is operable to supply a large current than said second current source [col. 8, lines 48-63].

21. As per claim 12, Nolan et al teach that wherein said first reference voltage is established across a resister [col. 8, lines 61-63].

22. As per claim 13, Nolan et al teach that wherein said second reference voltage is established across a diode-connected field effect transistor [Fig. 3; col. 3, lines 51-55].

23. As per claims 16-17, Nolan et al disclose the invention substantially. Nolan et al do not expressly disclose that first current generates a current of 2 micro amps and second current source generates a current of 100 nano amps. However, Nolan et al clearly disclose that the clock frequency of the first operating mode being lower than the clock frequency of the second operating mode [col. 8, lines 56-60]. Therefore, it would have been obvious to one of ordinary skill in the art at time the invention was made to have the first current source generating a current of 100 nano amps and second current source generating a current of 2 micro amps.

24. As per claims 18, Nolan et al disclose the invention substantially. Nolan et al do not expressly disclose that relaxation oscillator circuit generates a clock signal operating at a frequency of substantially 32 KHz. However, a routineer in the art would know that it is possible to clock the relaxation oscillator at a necessary clock according to the system requirement. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have the relaxation oscillator circuit generating a clock signal operating at frequency of substantially 32 KHz.

25. Claims14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nolan et al (US Patent no 6,052,035[1]), Schade, Jr. (US Patent No 4,250,464; hereinafter referred to as Schade) in view of May (US Patent No 5,426,384).

26. As per claim 14, Nolan and Schade disclose the invention substantially. Nolan and Schade do not disclose about trimmable current sources are being digitally controlled. However, May clearly discloses the knowledge of a voltage-controlled oscillator (VCO) having a voltage controlled current source that is digitally controlled. May also discloses that the VCO could be replaced by a relaxation oscillator [col. 5, liens 56-59; col. 9, lines 5-7]. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the cited references as they are directed to voltage controlled oscillator. Moreover, a digitally controlled current source can be controlled by a microcontroller or microprocessor. A digitally controlled current source is less susceptible to changes caused by environmental conditions.

27. As per claim15, Nolan et al clearly disclose having at least three trimmable current sources. Nolan et al do not disclose having four trimmable current sources. However, a routineer in the art would understand that it is possible in a different embodiment to have more than three trimmable current sources. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have more than three trimmable current sources. A routineer in the art would know that a greater number of trimmable current sources will provide a greater accuracy of the current but at the same time increase the amount of circuitry and control logic complexity.

Response to Arguments

28. Applicant's arguments with respect to claims 1-9 and 11-27 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Suresh K Suryawanshi whose telephone number is 571-272-3668. The examiner can normally be reached on 9:00am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

sks
April 4, 2005

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